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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/892,893	06/28/2001	Yoshikazu Ibara	010834	1585

23850 7590 10/10/2003

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EXAMINER	
COLEMAN, WILLIAM D	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 10/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/892,893	IBARA ET AL.	
	Examiner	Art Unit	
	W. David Coleman	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on July 25, 2003 has been entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

2. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

3. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Wieczorek et al., U.S. Patent 6,207,563.

4. Pertaining to claim 1, see **FIGS. 4-7**, where Wieczorek teaches a method for forming a silicide conductive structure on a semiconductor device, the method comprising:

depositing metal **66** on the surface of a patterned semiconductor film;

heat treating the semiconductor film on which the metal is deposited; removing residual metal that did not react during the heat treating step; and

repeating a sequence of the depositing step, the heat treating step, and the removing step once or a number of times. Please note that Wolf is incorporated by reference and specifically, Wolf discloses the repeating sequence step. (On page 140 of Wolf, second paragraph, TiSi2 is disclosed and an additional "thin layer of Ti is deposited". Wolf further discloses that "The underlying Ti forms a low resistance contact to the TiSi2 (since any native SiO2 on the silicide is consumed by reaction with the Ti), and the sputtered-W layer prevents the formation of the high-resistivity TiF3 layer on the TiSi2 during the CVD process").

5. Pertaining to claim 2, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 1, further comprising: heat treating the semiconductor film after the repeating step at a temperature that is higher than that of the heat treating step (column 6, lines 57-59 and column 7, lines 61-62).

6. Pertaining to claim 3, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 2, wherein the patterned semiconductor film is an N-type semiconductor (column 6, line 7).

7. Pertaining to claim 4, Wieczorek teaches a method for manufacturing a semiconductor device, comprising:

forming a conductive portion on a substrate, wherein the conductive portion includes a gate electrode; forming a spacer on a side wall of the gate electrode; depositing metal on the surface of the substrate including the conductive portion; applying silicide on the conductive portion in a self-aligned manner by heat treating the substrate on which the metal is deposited; removing residual metal that did not react during the heat treatment; and

repeating a sequence of the depositing step, the silicide applying step, and the removing step once or a number of times. (On page 140 of Wolf, second paragraph, TiSi2 is disclosed and an additional "thin layer of Ti is deposited". Wolf further discloses that "The underlying Ti forms a low resistance contact to the TiSi2 (since any native SiO2 on the silicide is consumed by reaction with the Ti), and the sputtered-W layer prevents the formation of the high-resistivity TiF3 layer on the TiSi2 during the CVD process").

8. Pertaining to claim 5, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 4, further comprising:

heat treating the substrate after the repeating step at a temperature that is higher than that of the heat treating

9. Pertaining to claim 6 Wieczorek teaches the method for manufacturing the semiconductor device according to claim 5, wherein the conductive portion to which silicide is applied is an N-type semiconductor.

10. Pertaining to claim 7, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 4, wherein the thickness of the

cm), and the gate electrode is 1,000 Å (10 cm) to 2,500Å (column 5, line 54) heat treating is repeated in a temperature range of 600^{0}C to 720^{0}C (column 6, line 59.

11. Pertaining to claim 8, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 7, further comprising:

heat treating the substrate after the repeating step for 30 seconds at a temperature of about 850^{0}C (column 7, lines 61-62).

12. Pertaining to claim 9, Wieczorek teaches the method for manufacturing the semiconductor device according to claim 8, wherein the conductive portion to which silicide is applied is an N-type semiconductor.

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 703-305-0004. The examiner can normally be reached on 9:00 AM-5:00 PM.

14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 703-306-2794. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

15. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

W. David Coleman
Primary Examiner
Art Unit 2823

WDC